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☐ 1. Document ID: US 6768577 B2

L10: Entry 1 of 16 File: USPT Jul 27, 2004

US-PAT-NO: 6768577
DOCUMENT-IDENTIFIER: US 6768577 B2

TITLE: TUNABLE MULTIMODE LASER DIODE MODULE, TUNABLE MULTIMODE WAVELENGTH DIVISION MULTIPLEX RAMAN PUMP, AND AMPLIFIER, AND A SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR CONTROLLING TUNABLE MULTIMODE LASER DIODES, RAMAN PUMPS, AND RAMAN AMPLIFIERS

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 2. Document ID: US 6753873 B2

L10: Entry 2 of 16 File: USPT Jun 22, 2004

US-PAT-NO: 6753873
DOCUMENT-IDENTIFIER: US 6753873 B2

TITLE: Shared memory control between detector framing node and processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 3. Document ID: US 6649914 B1

L10: Entry 3 of 16 File: USPT Nov 18, 2003

US-PAT-NO: 6649914
DOCUMENT-IDENTIFIER: US 6649914 B1

TITLE: Scanning-beam X-ray imaging system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 4. Document ID: US 6624524 B1

L10: Entry 4 of 16 File: USPT Sep 23, 2003

US-PAT-NO: 6624524
DOCUMENT-IDENTIFIER: US 6624524 B1

TITLE: Laser alignment target

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 5. Document ID: US 6504895 B2

L10: Entry 5 of 16 File: USPT Jan 7, 2003

US-PAT-NO: 6504895
DOCUMENT-IDENTIFIER: US 6504895 B2

TITLE: Method and system monitoring image detection

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 6. Document ID: US 6470071 B1

L10: Entry 6 of 16 File: USPT Oct 22, 2002

US-PAT-NO: 6470071
DOCUMENT-IDENTIFIER: US 6470071 B1

TITLE: Real time data acquisition system including decoupled host computer

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 7. Document ID: US 6333940 B1

L10: Entry 7 of 16 File: USPT Dec 25, 2001

US-PAT-NO: 6333940
DOCUMENT-IDENTIFIER: US 6333940 B1

TITLE: Integrated digital loop carrier system with virtual tributary mapper circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 8. Document ID: US 6049550 A

L10: Entry 8 of 16 File: USPT Apr 11, 2000

US-PAT-NO: 6049550
DOCUMENT-IDENTIFIER: US 6049550 A

TITLE: Integrated digital loop carrier system with virtual tributary mapper circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 9. Document ID: US 6002182 A

L10: Entry 9 of 16 File: USPT Dec 14, 1999

US-PAT-NO: 6002182
DOCUMENT-IDENTIFIER: US 6002182 A

TITLE: Laser alignment target

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

☐ 10. Document ID: US 5998295 A

L10: Entry 10 of 16 File: USPT Dec 7, 1999

US-PAT-NO: 5998295
DOCUMENT-IDENTIFIER: US 5998295 A

TITLE: Method of forming a rough region on a substrate

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

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Terms	Documents
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L10: Entry 10 of 16 File: USPT Dec 7, 1999

US-PAT-NO: 5998295
DOCUMENT-IDENTIFIER: US 5998295 A

TITLE: Method of forming a rough region on a substrate

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda U.	Sunnyvale	CA		

US-CL-CURRENT: 438/666; 148/DIG.20, 257/E23.15, 257/E23.179, 438/629, 438/672, 438/691, 438/964

Previous Doc Next Doc Go to Doc#

L10: Entry 10 of 16 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 5998295 A
TITLE: Method of forming a rough region on a substrate

Abstract Text (1):
A technique to form a structure with a rough topography (415) in a planarized semiconductor process. The rough topography (415) is formed by creating cored contacts (433). Subsequent process layers may be further stacked on top of the cored contacts in order to augment the nonplanar characteristics of the cored contacts. This rough topography structure may be used to align integrated circuits and wafers. An integrated circuit may be laser aligned using this alignment structure.

Brief Summary Text (3):
There are many circumstances where aligning a wafer or integrated circuit die is important. For example, alignment is important during the processing of integrated circuits. Integrated circuits are fabricated using a layer-by-layer process. Alignment may be critical during the processing of certain layers, where these layers must to aligned properly in relationship to previous layers. For example, a contact layer must be aligned properly with a first conductor layer in order to create contacts at the correct locations. Contacts formed at the wrong locations may create shorts or opens, and reduce yield.

Brief Summary Text (4):
Proper alignment is also critical in many other situations. These include testing of an integrated circuit die on a wafer. The die must be positioned properly in order to properly probe the device.

Brief Summary Text (5):
Moreover, alignment is also important when programming or configuring an integrated circuit. For example, a die may have fuses that are to be laser programmed. The fuses may be made of polysilicon, or another conductor. This fuse may couple together two (or more) devices or conductors. A laser with sufficient energy is directed at the fuse. The laser "blows" the fuse, decoupling the two devices or conductors. In order for the laser to properly reference the coordinates of a fuse, the integrated circuit must be aligned properly. When the integrated circuit is not aligned properly, the laser may damage or destroy a portion of the circuitry instead of blowing the desired fuse. Therefore, the alignment of an integrated circuit or wafer is especially critical.

Brief Summary Text (6):
A wafer or integrated circuit die may need to be aligned properly in an X-direction, Y-direction, rotation angle, and other orientation. As technology improves, alignment is becoming more important and critical, especially resulting from the continued scaling and shrinking of semiconductor device geometries. Integrated circuits (or "chips") have progressively become smaller and denser, and any small misalignment will adversely affect the integrated circuit yield and functionality of the integrated circuit.

Brief Summary Text (7):
One technique of alignment is by use of an alignment target. An alignment target

should have good reflective or optical contrast so it can be easily identifiable. For example, a laser may be used to determine a change in reflectivity or optical contrast in a semiconductor structure used as the alignment target. This contrast may be achieved by forming a region with rough topography and a region into a smooth topography, where these regions are in close proximity to one another. Light is reflected from the smooth or planar region while light is scattered from the rough region. A laser alignment system would find this alignment target and align the wafer or integrated circuit based on the target.

Brief Summary Text (9):
Despite the substantial success of such planarized process technologies, these processes also meet with certain limitations, especially when used to create a region having good reflectivity, which may be used as an alignment target. With flat or smooth topographies, the resulting structures and regions will have a similar optical reflectiveness. This leads to poor reflective or optical contrast, making it difficult (and possibly impossible) to align a wafer or integrated circuit die, especially by using laser. Furthermore, in some processes, metals use antireflective coatings, further reducing the reflectivity contrast over flat topography.

Brief Summary Text (10):
As can be seen, a structure and technique for fabricating a good reflective contrast is needed, especially where this structure is useful as an alignment target for aligning a wafer or integrated circuit.

Brief Summary Text (12):
The present invention is a structure and technique for fabricating a structure having good reflective contrast for use as an alignment structure. In particular, a technique of the present invention is for fabricating a structure having a rough topography using a planarized semiconductor process. The rough topography structure of present invention has a different reflectivity compared to a smooth or planar topography structure. Specifically, the rough topography will scatter incident radiation and light, while the smooth topography will reflect radiation and light. A structure including both rough and smooth topographies may be used as an alignment target for aligning an integrated circuit or wafer.

Brief Summary Text (13):
The system will be able to identify the reflective and optical contrast between the smooth and rough topography. After alignment, an integrated circuit, such as a memory, microprocessor, or programmable logic device, may be programmed, such as by a laser to blow laser-programmable fuses.

Brief Summary Text (16):
Moreover, an alignment structure for semiconductor fabrication of the present invention includes a smooth and a rough region formed on a substrate. The rough region includes a first conductive layer and a second conductive layer formed above the first conductive layer. A first insulating layer is formed between the first and second conductive layers. The first insulating layer has a first opening for electrically coupling the first and second conductive layers. A plug layer, having a cored region, fills the first opening. The topographical roughness formed by the cored region scatters incident radiation.

Drawing Description Text (2):
FIG. 1 shows alignment targets and an integrated circuit with programmable fuses;

Drawing Description Text (3):
FIG. 2A shows a top view of an alignment structure of the present invention;

Drawing Description Text (4):
FIG. 2B shows a top view of another embodiment of an alignment structure of the

present invention;

Drawing Description Text (6):
FIG. 4 shows a cross-section of an alignment structure of the present invention;

Detailed Description Text (2):
FIG. 1 is a diagram of an integrated circuit 110 and alignment targets 120. Integrated circuit 110 may be one of many on a wafer. Alignment targets 120 are used to align the integrated circuit. For example, alignment targets 120 may be used in the laser alignment of integrated circuit 110. Alignment targets 120 may also be used to align other objects and structures, such as entire wafers.

Detailed Description Text (3):
In the embodiment in FIG. 1, the alignment targets are shown as L-shaped structures. Many other shapes and sizes of alignment targets may be used including crosses ("X's"), pluses ("+'s"), and tees ("T's"), just to name a few. The shape and size of the structure are selected to permit easy and precise alignment.

Detailed Description Text (4):
For more precise alignment, the alignment targets should be positioned relatively close to the structure to be aligned. Specifically, in FIG. 1, alignment targets 120 are placed adjacent to, but outside integrated circuit 110. Moreover, for example, alignment targets 120 may be in a die seal or scribe line adjacent particular dies within a wafer.

Detailed Description Text (5):
In further embodiments of the present invention, the alignment targets may also be placed within integrated circuit 110. In some circumstances, this may be necessary because of the processing requirements. Further, this may be necessary, for example, when aligning integrated circuit dies which have already been sawed from the wafer. However, having alignment targets within the integrated circuit may be somewhat undesirable because it reduces the amount of usable area within the integrated circuit.

Detailed Description Text (6):
Alignment targets may be used to align multiple or groupings of integrated circuit dies at the same time. For example, an array of two rows by three columns of integrated circuit dies may use the same set of alignment targets. Since more than one die may be "group aligned" simultaneously, this approach may save time when aligning the integrated circuits. Also, since fewer alignment targets are needed, less area is used by the alignment targets, so more dies may be placed on a wafer. This technique may be used in a multiple-die reticle field. As all the die in a reticle field are exposed at one time, there is no relative variation between the die. However, different reticle steppings may have movement variations; then, separate alignment is typically required.

Detailed Description Text (7):
For alignment, a pair of alignment targets may be used, such as shown in FIG. 1. However, there may be any number of alignment targets, sufficient to allow for precise and accurate alignment. The integrated circuit may need to be aligned in several different directions and angles, including, for example, an X-direction, Y-direction, and rotation angle. The number and shape of the alignment targets should be selected to allow the desired alignment approach.

Detailed Description Text (8):
A particular application, among many others, where alignment of integrated circuits is especially important is the laser programming of fuses within the dies. As shown in FIG. 1, there may be one of more fuses 130 within the integrated circuit. Each may control a particular feature. For example, fuse-programmable options may be used to repair against low-level defects in integrated circuits. If a defect is

L10: Entry 9 of 16 File: USPT Dec 14, 1999

DOCUMENT-IDENTIFIER: US 6002182 A
TITLE: Laser alignment target

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Brief Summary Text (5):
Moreover, alignment is also important when programming or configuring an integrated circuit. For example, a die may have fuses that are to be laser programmed. The fuses may be made of polysilicon, or another conductor. This fuse may couple together two (or more) devices or conductors. A laser with sufficient energy is directed at the fuse. The laser "blows" the fuse, decoupling the two devices or conductors. In order for the laser to properly reference the coordinates of a fuse, the integrated circuit must be aligned properly. When the integrated circuit is not aligned properly, the laser may damage or destroy a portion of the circuitry instead of blowing the desired fuse. Therefore, the alignment of an integrated circuit or wafer is especially critical.

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A wafer or integrated circuit die may need to be aligned properly in an X-direction, Y-direction, rotation angle, and other orientation. As technology improves, alignment is becoming more important and critical, especially resulting from the continued scaling and shrinking of semiconductor device geometries. Integrated circuits (or "chips") have progressively become smaller and denser, and any small misalignment will adversely affect the integrated circuit yield and functionality of the integrated circuit.

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Despite the substantial success of such planarized process technologies, these processes also meet with certain limitations, especially when used to create a region having good reflectivity, which may be used as an alignment target. With flat or smooth topographies, the resulting structures and regions will have a similar optical reflectiveness. This leads to poor reflective or optical contrast, making it difficult (and possibly impossible) to align a wafer or integrated circuit die, especially by using laser. Furthermore, in some processes, metals use antireflective coatings, further reducing the reflectivity contrast over flat topography.

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As can be seen, a structure and technique for fabricating a good reflective contrast is needed, especially where this structure is useful as an alignment target for aligning a wafer or integrated circuit.

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The present invention is a structure and technique for fabricating a structure having good reflective contrast for use as an alignment structure. In particular, a technique of the present invention is for fabricating a structure having a rough topography using a planarized semiconductor process. The rough topography structure of present invention has a different reflectivity compared to a smooth or planar topography structure. Specifically, the rough topography will scatter incident radiation and light, while the smooth topography will reflect radiation and light. A structure including both rough and smooth topographies may be used as an alignment target for aligning an integrated circuit or wafer. The system will be able to identify the reflective and optical contrast between the smooth and rough topography. After alignment, an integrated circuit, such as a memory, microprocessor, or programmable logic device, may be programmed, such as by a laser to blow laser-programmable fuses.

Brief Summary Text (15):
Moreover, an alignment structure for semiconductor fabrication of the present invention includes a smooth and a rough region formed on a substrate. The rough region includes a first conductive layer and a second conductive layer formed above the first conductive layer. A first insulating layer is formed between the first and second conductive layers. The first insulating layer has a first opening for electrically coupling the first and second conductive layers. A plug layer, having a cored region, fills the first opening. The topographical roughness formed by the cored region scatters incident radiation.

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FIG. 2A shows a top view of an alignment structure of the present invention;

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Drawing Description Text (7):
FIG. 4 shows a cross-section of an alignment structure of the present invention;

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In further embodiments of the present invention, the alignment targets may also be placed within integrated circuit 110. In some circumstances, this may be necessary because of the processing requirements. Further, this may be necessary, for example, when aligning integrated circuit dies which have already been sawed from the wafer. However, having alignment targets within the integrated circuit may be somewhat undesirable because it reduces the amount of usable area within the integrated circuit.

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Detailed Description Text (7):
For alignment, a pair of alignment targets may be used, such as shown in FIG. 1. However, there may be any number of alignment targets, sufficient to allow for precise and accurate alignment. The integrated circuit may need to be aligned in several different directions and angles, including, for example, an X-direction, Y-direction, and rotation angle. The number and shape of the alignment targets should be selected to allow the desired alignment approach.

Detailed Description Text (8):
A particular application, among many others, where alignment of integrated circuits is especially important is the laser programming of fuses within the dies. As shown in FIG. 1, there may be one of more fuses 130 within the integrated circuit. Each may control a particular feature. For example, fuse-programmable options may be used to repair against low-level defects in integrated circuits. If a defect is found in a particular circuit, then after the integrated circuit has been aligned using the alignment targets, a laser is referenced to a selected fuse location with

the integrated circuit. The laser "blows" the fuse, which may be made of polysilicon or metal, in order to enable or disable the appropriate circuitry.

Detailed Description Text (9):
Alignment is especially critical since the laser must properly reference the precise location on the integrated circuit to program the fuse. For example, fuses may occupy less than 100 square micron area. Any misalignment error, and the laser may damage a portion of the integrated circuit.

Detailed Description Text (10):
Laser programming may also be employed in implementing redundancy of integrated circuit chips. With redundancy, some defective elements of a die can be replaced with nondefective extra resources provided for the repair. The accuracy of the replacement depends on the accuracy of laser programming.

Detailed Description Text (11):
Laser programming may be useful for configuring various types of integrated circuits including, but not limited to, memories, microprocessor, ASICs, gate arrays, field programmable gate arrays (FPGAs), and programmable logic devices (PLDs). For example, for PLDs, laser programming may be used to configure the logical elements and interconnections within between the logical elements. PLDs are typically programmed by electrically programming fuses, antifuses, EPROM, Flash, EEPROM, or SRAM cells.

Detailed Description Text (13):
Laser programming may be used in place of, or to supplement, the electrical configuration of PLDs. For example, laser programming may be used to program the programmable interconnect array (PIA), global interconnect, local interconnect, and other interconnection within a PLD. Laser programming may also be used to configure the functionality of logic array blocks (LABs) and logic elements (LEs). As a further example, a look-up table in a PLD may be configured by the way of laser programming.

Detailed Description Text (14):
The integrated circuit may be programmed in part by laser programming, then further electrically configured or programmed by a user. The user may program the device using a programmer device or using in-system programming (ISP). ISP involves electrically programming an integrated circuit while it resides on a system board. For example, a laser may program a portion of the global interconnect; and if desirable or necessary, the remaining portion of the global interconnect is configured in the field (i.e., by a customer or user).

Detailed Description Text (15):
Laser programming may be used to implement some features which are typically implemented using mask-programmable options. Mask-programmable options are features of the integrated circuit which are enabled or disabled by using an appropriate mask,during a masking step. These options are usually implemented during a metal masking step, such as first or second metal layers. Although mask-programmable options are an effective technique, laser programming offers many advantages. For example, among other advantages, laser programming may lower overall production cost since integrated circuit dies do not need to be laser programmed until just before the parts are needed. Generic (unconfigured) parts may be stored in inventory and laser configured as needed. This eliminates the need of keeping an inventory in various customized and specialized products.

Detailed Description Text (16):
FIG. 2A shows an embodiment of an alignment target 210 of the present invention. Here, alignment target 210 is an "L" shape; however, as discussed above, the alignment target may be many other shapes. Alignment target 210 may be mirrored, rotated, and positioned as desired on the wafer or integrated circuit.

Detailed Description Text (17):
Alignment target 210 includes a rough topography 220 and a smooth topography 230. Rough topography 220 and smooth topography 230 have a dissimilar optical reflectiveness. Generally, smooth topography 230 reflects incident radiation or light while rough topography 220 scatters incident radiation or light. Furthermore, on a wafer, especially one processed using a planarized process, areas (e.g., substrate, active regions) other than rough topography 220 will generally be highly reflective regions like smooth topography 230.

Detailed Description Text (18):
FIG. 2B illustrates an alternative embodiment of the alignment structure. In this embodiment compared to FIG. 2A, rough topography regions 220 are reversed with smooth topography regions 230. Use and fabrication of this alignment structure would be analogous to that for the structure shown in FIG. 2A.

Detailed Description Text (19):
An alignment system (which may use a laser) scans alignment target 210 and can recognize a difference in reflectivity between rough topography 220 and smooth topography 230. Using alignment target 210, the alignment system makes adjustments to position the wafer or integrated circuit into proper alignment. For example, a laser may scan alignment target 210 along a line and direction from 250 to 255. While scanning the alignment target, the scanning instruments will detect the difference in reflectivity between rough topography 220 and smooth topography 230. The reflectivity changes at an interface 270 between rough topography 220 and smooth topography 230.

Detailed Description Text (20):
In addition, there should be adequate space around the alignment mark so that circuitry or other features may not be mistaken for the alignment mark. Furthermore, the laser alignment may scan multiple times, such as in the X and Y directions. And, there may be multiple scan marks. In a preferred embodiment, three alignment marks are used. A more precise alignment will result when using four or more targets.

Detailed Description Text (24):
Plug layer 330 helps produce a flatter topography. Compared to a process without a plug layer, a step 350 between plug 330 and oxide 310 is minimized. Therefore, the resulting topography is smoother and flatter. As a result, subsequent layers stacked over plug layer 330, oxide 310, and step 350 will also be smoother and more planar. In some processes, the topography may even be planarized further by chemical-mechanical polishing (CMP), where the surface of oxide layer 310 is polished (or ground) to ensure its flatness. Therefore, using a planar process, its becomes increasingly difficult to create a rough regions on layer 340 which may be used as an alignment target.

Detailed Description Text (26):
FIG. 4 shows a cross-sectional view of alignment target 230 along the line 250 to 255 of FIG. 2A. A region with rough topography 410 has on either side, regions with smooth topography 415. This rough topography structure may be formed using a planarized process.

Detailed Description Text (40):
The structure and typically the entire wafer is covered with a passivation or insulating layer 468. Layer 468 may be a single layer material such as oxynitride, or multiple layers of material such as oxide, nitride, and polyimide. Passivation layer 468 may have cracks (not shown) over the cored regions 465. Passivation layer 468 over the alignment structure may be removed to enhance the difference in the reflectivity between the smooth and rough regions. In a specific embodiment, the passivation is removed from over rough region. This process also removes an

antireflective coating 463 from the metal enhancing reflectivity from smooth topography regions.

Detailed Description Text (41):
The topographically rough region formed, as described above, will scatter incident radiation, in contrast to a topographically smooth region, which reflects light. This difference in reflectivity, or reflectivity contrast, may be used by an alignment system for aligning integrated circuits and wafers.

Detailed Description Text (43):
For example, although described for a three-layer metal process, the technique and structure of the present invention will be equally applicable to a single-metal and double-metal process. In those cases, the contact layer is cored, and subsequent via layers, if any, are also cored. This would result in structure with a rough topography useful for an alignment structure.

Detailed Description Text (44):
Furthermore, varying degrees of contrast in reflectivity may be achieved by selecting or limiting the number of layers which are cored. For example, in a three-layer metal process, only the via-1 layer may be cored to create a region with a first degree of reflectivity. In another region, the contact and via-1 layers may be cored to create a second degree of reflectivity. An alignment system may use these varying degrees of reflectivity for more precise alignment of the integrated circuit.

Other Reference Publication (1):
TLSI "Design Guidelines for Laser Fusing of ID Tags," Feb. 19, 1991, 7 pages.

Other Reference Publication (3):
Article in E E Times, "DAC Briefs: Chip Express Introduces Laser-Programming Arrays," Jun. 10, 1996, 1 page.

Other Reference Publication (5):
Chip Express Press Release, "The Chip Express QYH500 Laser Gate Array (LPGA) Family Now Supports 3-Volt Custom Designs," Santa Clara, CA, May 17, 1996, 1 page.

Other Reference Publication (6):
Chip Express Press Release, "Chip Express Unviels a 200,000 Gate LPGA Family with Configurable Embedded SRAM: The CX2000 New Gate Array Architecture Eases Deep Sub-micron Designs," Las Vegas, NV, Jun. 3, 1996, 2 pages.

Other Reference Publication (7):
Chip Express Press Release, "Chip Express Annouces Low-Production Volumn OneMask.RTM. Gate Arrays Screened to Military Standard 883: Rapid-Turn Laser-Prototyping Used by the Military," Santa Clara, CA, Aug. 21, 1995, 2 pages.

Other Reference Publication (11):
Smith, et al., "Laser Programmable Redundancy and Yield Improvement in a 64K DRAM," IEEE Journal of Solid-State Circuits, vol. SC-16, No. 5, Oct. 1981, pp. 506-513.

CLAIMS:

1. An alignment structure formed in a planarized semiconductor process comprising:

a substrate;

a contact opening formed on the substrate;

a first plug layer filling the contact opening, the first plug layer having a first depressed region in the contact opening, whereby a topological roughness formed by

the first depressed region scatters incident radiation.

2. The alignment structure of claim 1 wherein the topological roughness contrasts reflectively to a topographically smooth region.

3. The alignment structure of claim 1 wherein the first depressed region is in about a middle of the contact opening.

4. The alignment structure of claim 1 further comprising:

a first via opening stacked on top of the contact opening, whereby the first via opening enhances the topological roughness formed by the first depressed region.

5. The alignment structure of claim 1 wherein the contact opening is larger than a minimum size specified by a design rule.

6. The alignment structure of claim 4 further comprising:

a second via opening stacked on top of the first via opening and second via opening, whereby the second via opening further enhances the topological roughness.

7. An alignment structure for semiconductor fabrication comprising:

a smooth region formed on a substrate;

a rough region formed on the substrate comprising:

a first conductive layer;

a second conductive layer formed above the first conductive layer,

an first insulating layer, between the first and second conductive layers, wherein the first insulating layer has a first opening for electrically coupling the first and second conductive layers;

a plug layer filling the first opening, wherein the first plug layer has a cored region, whereby a topological roughness formed by the cored region scatters incident radiation.

8. The alignment structure of claim 7 wherein the rough region further comprises:

a third conductive layer formed above the second conductive layer;

a second insulating layer, between the second and third conductive layers, wherein the second conductive layer has a second opening, stacked above the first opening, for electrically coupling the third and second conductive layers, whereby the second opening aggravates the topological roughness formed by the cored region.

9. The alignment structure of claim 7 wherein the cored region creates a void above the cored region and second conductive layer.

10. The alignment structure of claim 8 wherein the opening has a lateral dimension at least about 1.5 times larger than a minimum size.

11. The alignment structure of claim 8 wherein a passivation layer, covering the substrate, is removed from the rough region to enhance a reflectivity contrast between the rough region and smooth region.

12. The alignment structure of claim 8 wherein the smooth region is adjacent to the

rough region.

13. The alignment structure of claim 8 wherein the smooth region is formed using a metal layer.

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US-PAT-NO: 6002182
DOCUMENT-IDENTIFIER: US 6002182 A

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INVENTOR-INFORMATION:

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